Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A circuit ~~comprising~~comprising:

a first terminal that outputs an operating point;

a first circuit group charging the first terminal;

a second circuit group discharging the first terminal;

an applying portion applying a weighted mean of a plurality of inputs to one or both of the first circuit group and the second group;

a spin transistor having transfer characteristics depending on the spin direction of conduction ~~carriers,~~carriers and being included in one or both of the first circuit group and the second circuit group; and

an output terminal that outputs a Boolean function of a plurality of inputs based on the operating point, wherein

~~the spin direction of the conduction carriers being changed so as to vary the transfer characteristics of the spin transistor,~~

~~an operating~~ the operating point ~~being~~ is changed based on the transfer characteristics, thereby reconfiguring ~~a function.~~the Boolean function.

2. (Currently Amended) ~~A circuit comprising~~The circuit as claimed in claim 1, wherein:

~~a spin transistor that~~the spin transistor includes at least two ferromagnetic layers, and ~~has~~ has the transfer characteristics depending on ~~on the~~ magnetization ~~state~~ states of the ferromagnetic ~~layers,~~ layers; and

the magnetization ~~state~~ states of the spin transistor ~~being changed to move an~~ is changed to move the operating point, thereby reconfiguring ~~a function.~~ the Boolean function.

3. (Currently Amended) The circuit as claimed in claim 2, wherein:

the spin transistor has at least one ferromagnetic body ("free layer") with a magnetization direction that can be controlled independently, and at least one ferromagnetic body ("pin layer") with a fixed magnetization direction; and

~~the circuit reconfigures a function by changing an~~the spin transistor changes the operating point based on two of the magnetization states including a first state in which the free layer and the pin layer have the same magnetization directions ("parallel magnetization"), and a second state in which the free layer and the pin layer have the opposite magnetizing states to each other ("antiparallel magnetization").

4. (Canceled)

5. (Currently Amended) The circuit as claimed in ~~claim 4,~~ claim 1, wherein the first terminal has a potential that is determined by changing the spin directions of the condition carriers of the spin transistor or by controlling the transfer characteristics depending ~~on the~~ on magnetization state of the spin transistor.

6. (Currently Amended) The circuit as claimed in claim 1, ~~which outputs a signal based on a signal that is input via~~ wherein the applying portion has a neuron MOS (vMOS) structure ~~including a plurality of inputs weighted with capacitances by capacitors and a floating gate connecting the inputs.~~including capacitors weighing the plurality of inputs with capacitance thereof and a floating gate connecting weighted input signals.

7. (Currently Amended) The circuit as claimed in claim 6, wherein the weighted input signals are weighted so as to be substantially equal to one another.

8. (Currently Amended) The circuit as claimed in ~~claim 4,~~ claim 1, wherein a logic threshold value for dividing ~~the~~ a potential generated in the first terminal into an output of a logic level "0" and an output of a logic level "1" is set with respect to the operating point that varies according to a variation in the transfer characteristics of the spin transistor.

9. (Previously Presented) The circuit as claimed in claim 1, wherein an A-D converter with a predetermined logic threshold value is connected to an output terminal of the circuit.

10. (Previously Presented) The circuit as claimed in claim 1, wherein the spin transistor is a MOSFET-type spin transistor ("spin MOSFET") that are formed with a source and a drain, including a MOS structure and a ferromagnetic body.

11. (Currently Amended) The circuit as claimed in ~~claim 3,~~ claim 1, wherein the first circuit group includes a MOSFET of a first conductivity type or a spin MOSFET of the first conductivity type, and the second circuit group includes a MOSFET of the same conductivity type as the first conductivity type or a spin MOSFET of the same conductivity type as the first conductivity type.

12. (Currently Amended) The circuit as claimed in ~~claim 3,~~ claim 1, comprising an E/E circuit that includes a structure in which ~~the~~ a source of an enhancement MOSFET or an enhancement spin MOSFET contained in the first circuit group is connected to ~~the~~ a drain of an enhancement MOSFET or an enhancement spin MOSFET contained in the second circuit group, and a first terminal that is formed at the connection portion.

13. (Currently Amended) The circuit as claimed in claim 12, wherein the drain of ~~an~~ the enhancement MOSFET or ~~an~~ the enhancement spin MOSFET contained in the first circuit group in the E/E circuit is connected to ~~the~~ a gate of the enhancement MOSFET or the enhancement spin MOSFET.

14. (Currently Amended) The circuit as claimed in claim 12, wherein ~~an~~ the enhancement MOSFET or ~~an~~ the enhancement spin MOSFET contained in the second circuit group in the E/E circuit has a vMOS structure.

15. (Currently Amended) The circuit as claimed in ~~claim 3,~~ claim 1, comprising

an E/D circuit that includes a structure in which ~~the~~ a source of a depletion MOSFET or a depletion spin MOSFET contained in the first circuit group is connected to ~~the~~ a drain of an enhancement MOSFET or an enhancement spin MOSFET contained in the second circuit group, and a first terminal that is formed at the connection portion.

16. (Currently Amended) The circuit as claimed in claim 15, wherein the source of ~~a~~ the depletion MOSFET or ~~a~~ the depletion spin MOSFET contained in the first circuit group in the E/D circuit is connected to ~~the~~ a gate of the depletion MOSFET or the depletion spin MOSFET.

17. (Currently Amended) The circuit as claimed in claim 15, wherein ~~an~~ the enhancement MOSFET or ~~an~~ the enhancement spin MOSFET contained in the second circuit group in the E/D circuit has a vMOS structure.

18. (Currently Amended) The circuit as claimed in ~~claim 11,~~ claim 14, wherein the vMOS structure has two inputs (A and B) weighted with capacitances by capacitors.

19. (Currently Amended) The circuit as claimed in ~~claim 4,~~ claim 1, wherein the circuit is a NAND/NOR reconfigurable logic circuit or an AND/OR reconfigurable logic circuit that includes ~~the~~ a A-D converter having the first terminal as an input.

20. (Withdrawn-Currently Amended) The circuit as claimed in claim 11, wherein the first and second circuit groups or one of the first and second circuit groups comprises

a circuit that controls ~~the~~ a potential of the first terminal by connecting ~~the~~ a source or ~~the~~ a drain of another spin MOSFET to the first terminal, and connecting a level

shift circuit to ~~the~~ a gate of the another spin MOSFET, the level shift circuit turning on the another spin MOSFET only when a predetermined input is made.

21. (Withdrawn-Currently Amended) The circuit as claimed in claim 11, wherein the second circuit group comprises

a circuit that controls ~~the~~ a potential of the first terminal by connecting ~~the~~ a drain of another spin MOSFET of n-channel type to the first terminal, and connecting a level shift circuit to ~~the~~ a gate of the another spin MOSFET of n-channel type, the another spin MOSFET of n-channel having ~~the~~ a source grounded, the level shift circuit turning on the another spin MOSFET of n-channel type only when an input is A = B = "0".

22. (Withdrawn-Currently Amended) The circuit as claimed in claim 11, wherein the first circuit group comprises

a circuit that controls ~~the~~ a potential of the first terminal by connecting ~~the~~ a drain of another spin MOSFET of p-channel type to the first terminal, and connecting a level shift circuit to ~~the~~ a gate of the another spin MOSFET of p-channel type, the another spin MOSFET of p-channel having ~~the~~ a source connected to a supply voltage, the level shift circuit turning on the another spin MOSFET of p-channel type only when an input is A = B = "1".

23. (Withdrawn) The circuit as claimed in claim 20, wherein the level shift circuit is formed with an E/E, E/D, or CMOS inverter.

24. (Withdrawn-Currently Amended) The circuit as claimed in claim 20, wherein the circuit is a reconfigurable logic circuit that includes ~~the~~ an A-D converter having the first terminal as an input.

25. (Withdrawn-Currently Amended) The circuit as claimed in claim 20, wherein the circuit is a reconfigurable logic circuit that includes an inverter having ~~the~~ an output of ~~the~~ an A-D converter as an input, and can achieve all symmetric Boolean functions.

26. (Currently Amended) The circuit as claimed in ~~claim 3,~~ claim 1, wherein the first circuit group includes a MOSFET of a first conductivity type or a spin MOSFET of the first conductivity type, and the second circuit group includes a MOSFET of a second conductivity type different from the first conductivity type or a spin MOSFET of the second conductivity type.

27. (Original) The circuit as claimed in claim 26, comprising

a CMOS circuit that includes a structure in which a p-channel MOSFET or a p-channel spin MOSFET contained in the first circuit group is connected to an n-channel MOSFET or an n-channel spin MOSFET contained in the second circuit group with a shared drain terminal, and a first terminal that is formed at the shared drain terminal.

28. (Original) The circuit as claimed in claim 26, comprising

a CMOS circuit that is formed with a p-channel spin MOSFET contained in the first circuit group and an n-channel spin MOSFET contained in the second circuit group.

29. (Previously Presented) The circuit as claimed in claim 26, wherein the p-channel MOSFET or the p-channel spin MOSFET, and the n-channel MOSFET or the n-channel spin MOSFET of the CMOS circuit have a shared floating gate forming a νMOS structure.

30. (Original) The circuit as claimed in claim 29, wherein the νMOS structure has two inputs (A and B) weighted with capacitances by capacitors.

31. (Withdrawn) The circuit as claimed in claim 26, wherein the circuit is an AND/OR reconfigurable logic circuit or a NAND/NOR reconfigurable logic circuit that includes an A-D converter having the first terminal as an input.

32. (Withdrawn-Currently Amended) The circuit as claimed in claim 26, wherein the first and second circuit groups, or one of the first and second circuit groups comprises

a circuit that controls ~~the~~ a potential of the first terminal by connecting ~~the~~ a source or ~~the~~ a drain of another spin MOSFET to the first terminal, and connecting a level shift circuit to ~~the~~ a gate of the another spin MOSFET, the level shift circuit turning on the another spin MOSFET only when a predetermined input is made.

33. (Withdrawn-Currently Amended) The circuit as claimed in claim 26, wherein the second circuit group comprises

a circuit that controls ~~the~~ a potential of the first terminal by connecting ~~the~~ a drain of another spin MOSFET of n-channel type to the first terminal, and connecting a level shift circuit to ~~the~~ a gate of the another spin MOSFET of n-channel type, the another spin MOSFET of n-channel having ~~the~~ a source grounded, the level shift circuit turning on the another spin MOSFET of n-channel type only when an input is A = B = "0".

34. (Withdrawn) The circuit as claimed in claim 26, wherein the circuit is an AND/OR/XNOR reconfigurable logic circuit or a NAND/NOR/XOR reconfigurable logic circuit that includes an A-D converter having the first terminal as an input.

35. (Withdrawn) The circuit as claimed in claim 26, wherein the first circuit group comprises

a circuit that controls the potential of the first terminal by connecting the drain of the another spin MOSFET of p-channel type to the first terminal, and connecting a level shift circuit to the gate of the another spin MOSFET of p-channel type, the another spin MOSFET of p-channel having the source connected to a supply voltage, the level shift circuit turning on the another spin MOSFET of p-channel type only when an input is A = B = "1".

36. (Withdrawn) The circuit as claimed in claim 26, wherein the circuit is an AND/OR/XOR reconfigurable logic circuit or a NAND/NOR/XNOR reconfigurable logic circuit that includes an A-D converter having the first terminal as an input.

37. (Withdrawn-Currently Amended) The circuit as claimed in claim 26, wherein the circuit is a reconfigurable logic circuit that includes an inverter having ~~the~~ an output of ~~the~~ an A-D converter as an input, and can achieve all symmetric Boolean functions.

38. (Withdrawn-Currently Amended) The circuit as claimed in claim 26, wherein the circuit is formed with a circuit group that is characterized by:

controlling ~~the~~ a potential of the first terminal by connecting ~~the~~ a drain of another spin MOSFET of n-channel type to the first terminal, and connecting a level shift circuit to ~~the~~ a gate of the another spin MOSFET of n-channel type, the another spin MOSFET of n-channel having ~~the~~ a source grounded, the level shift circuit turning on the another spin MOSFET of n-channel type only when an input is A = B = "1"; and

controlling the potential of the first terminal by connecting ~~the~~ a drain of another spin MOSFET of p-channel type to the first terminal, and connecting a level shift circuit to ~~the~~ a gate of the another spin MOSFET of p-channel type, the another spin MOSFET of p-channel having ~~the~~ a source connected to a supply voltage, the level shift circuit turning on the another spin MOSFET of p-channel type only when an input is A = B = "0".

39. (Withdrawn) The circuit as claimed in claim 38, wherein the circuit is an all symmetric Boolean function logic circuit that includes an A-D converter having the first terminal as an input.

40. (Withdrawn) The circuit as claimed in claim 32, wherein the level shift circuit is formed with an E/E, E/D, or CMOS inverter.

41. (Withdrawn) An A-D converter comprising

a CMOS inverter,

one of a p-channel MOSFET or an n-channel MOSFET of the CMOS inverter being a spin MOSFET, or a p-channel MOSFET and an n-channel MOSFET of the CMOS inverter being spin MOSFETs.

42. (Withdrawn-Currently Amended) The A-D converter as claimed in claim 41, wherein a logic threshold value can be changed according to ~~the~~ a magnetization state of the spin MOSFET.

43. (Withdrawn) A logic circuit comprising

an A-D converter that has a variable logic threshold value and is connected to an output stage of a circuit having an analog output, the logic circuit being capable of reconfiguring a logic function.

44. (Canceled)

45. (Currently Amended) An integrated circuit comprising

the circuit ~~as claimed in claim 1.~~including:

a first terminal that outputs an operating point;

a first circuit group charging the first terminal

a second circuit group discharging the first terminal;

an applying portion applying a weighted mean of a plurality of inputs to one or both of the first circuit group and the second circuit group;

a spin transistor having transfer characteristics depending on the spin direction of conduction carriers and being included in one or both of the first circuit group and the second circuit group; and

an output terminal that outputs a Boolean function of a plurality of inputs based on the operating point, wherein

the operating point is changeable based on the transfer characteristics thereby reconfiguring the Boolean function.